

Development and deployment of Artificial Intelligence algorithms for CTAO Telescopes









AstroHEP-PPCC: Tecnologías Avanzadas para la Exploración del Universo y sus Componentes (TAU-CM)

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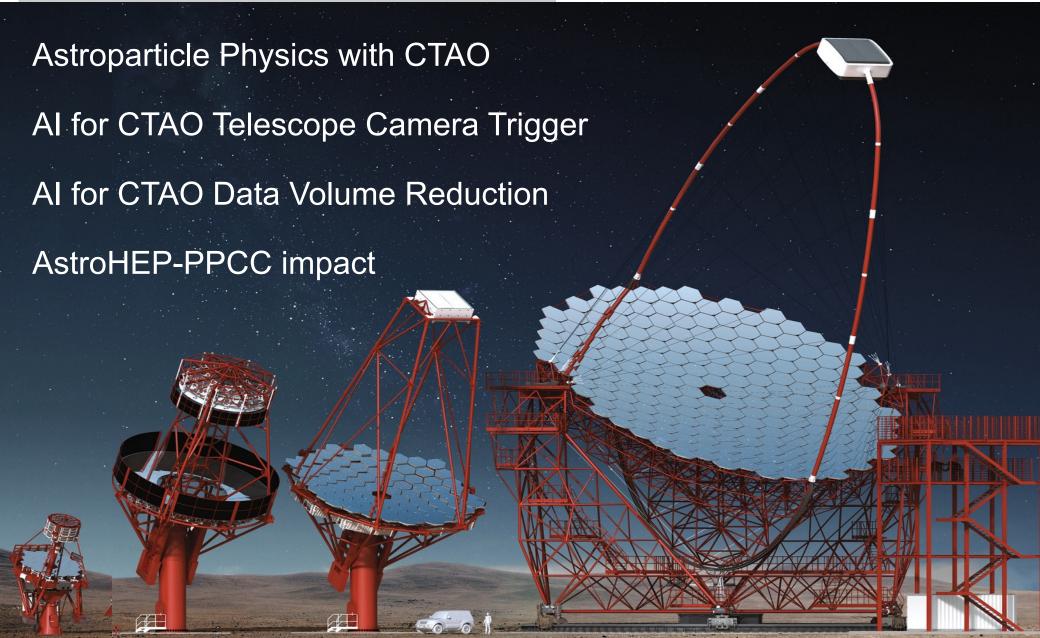






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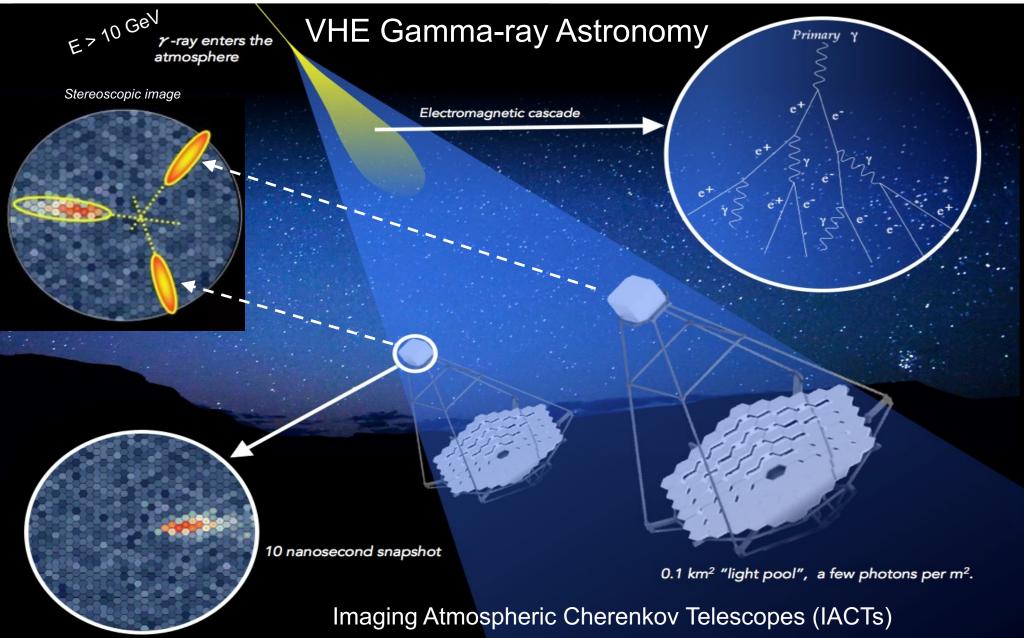






Astroparticle Physics











Cherenkov Telescope Array Observatory



Sensitivity improvement x10
Energy range extension x10
Angular resolution improvement



Two observatories:

La Palma / Chile ~100 telescopes







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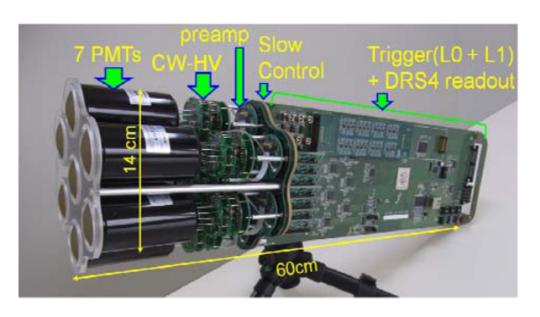






Cherenkov Telescope Array Observatory



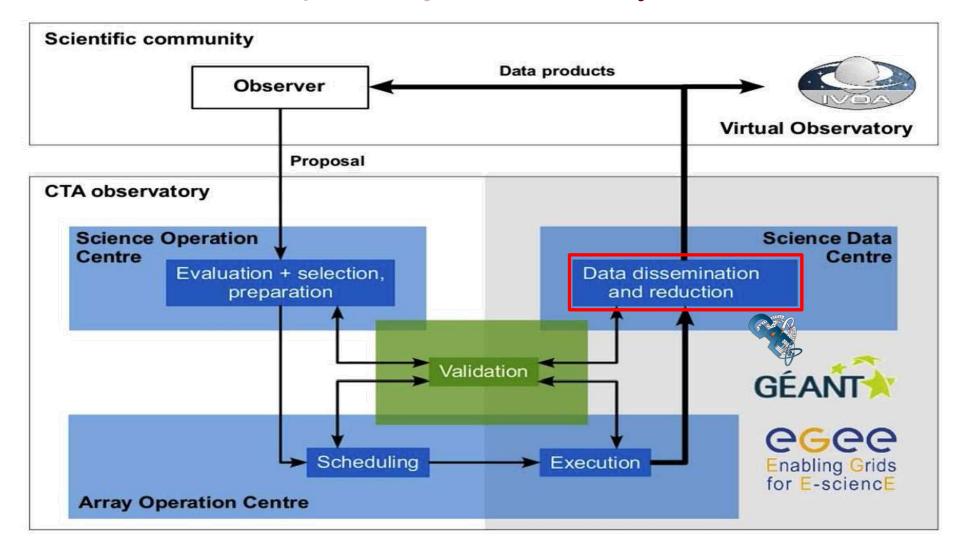


~2000 PMT-based camera





Cherenkov Telescope Array Observatory

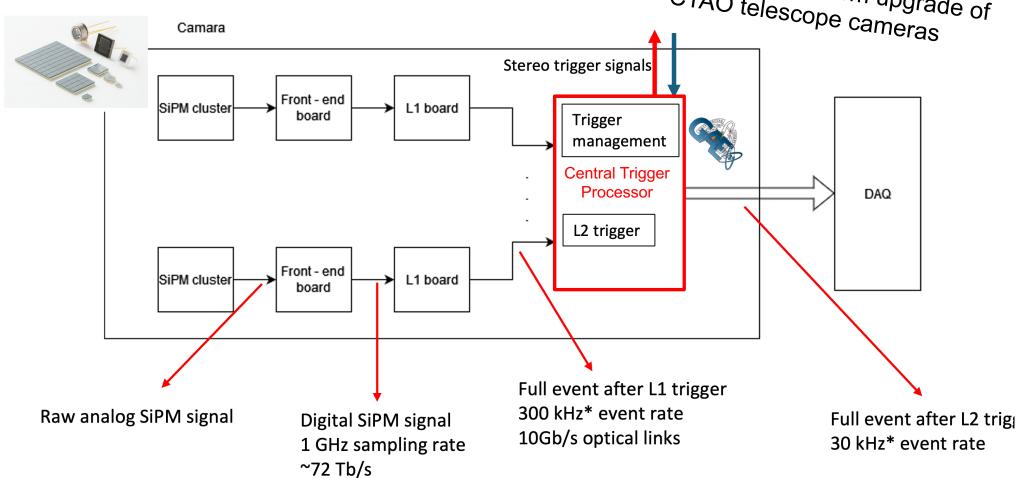






Advanced LST SiPM Camera*

Candidate for mid-term upgrade of CTAO telescope cameras

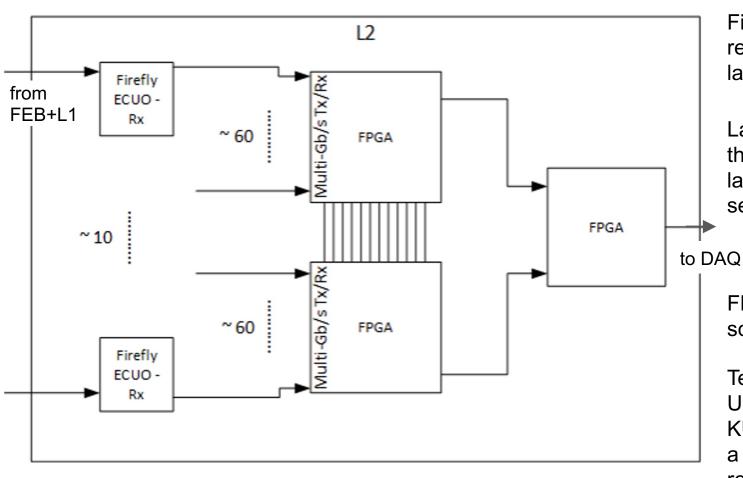


*PoS(ICRC2023)740





Central Trigger Processor: Al-based L2 trigger on FPGAs



First layer of FPGAs for data reception, formatting and first layers of CNN algorithm.

Last FPGA will take care of the CNN last fully connected layers, Event Building and sending the data to DAQ.

FPGAs in layers to allow scalability

Tentative FPGA models: Kintex UltraScale KU085, KU095 or KU115, with moderate cost and a large number of high-speed resources.

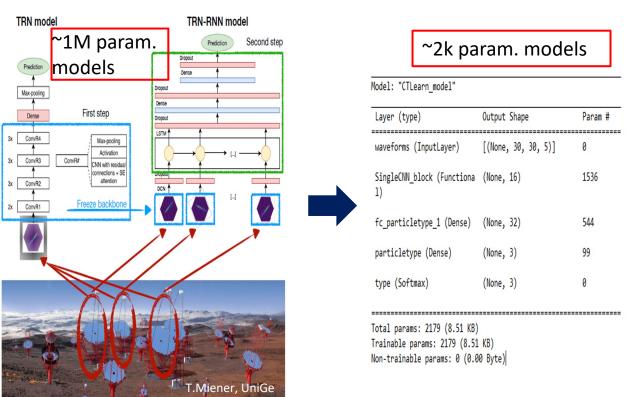


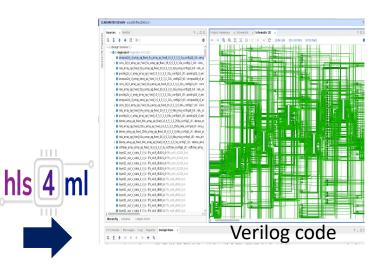




Al algorithms for CTAO camera trigger

- CTLearn*, led by IPARCOS-UCM members, builds CNN models for IACT array-based gamma/hadron/Night-Sky-Background separation
- Train small CNNs to fit in FPGAs → promising telescope-based shower/NSB separation
- Translating CNN models to firmware code







*https://github.com/ctlearn-project/ctlearn





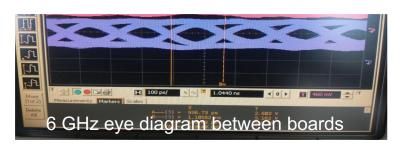


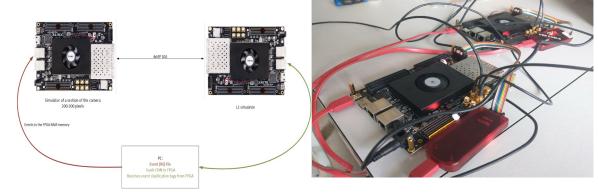
Prototype 1: CNN4FPGA trigger testbench

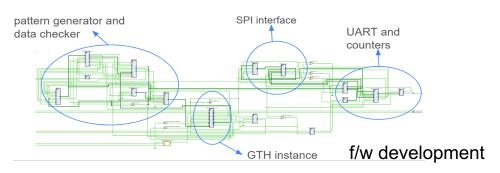
- Building the testbench
 - 2 development boards with Kintex UltraScale tier FPGAs (Alinx XCKU040 with 4 SFPs)
 - One board to simulate pixel data information (i.e. FEB+L1) and the other to implement & test firmware core and L2 algorithms

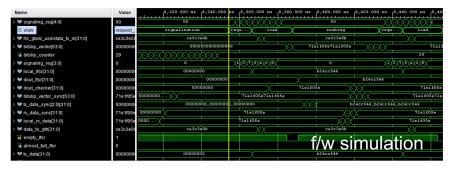
Using the testbench

- Develop f/w for multi-gigabit transceivers and other interfaces.
- Test f/w in the development boards.









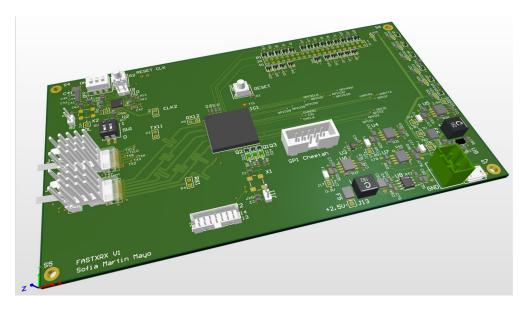


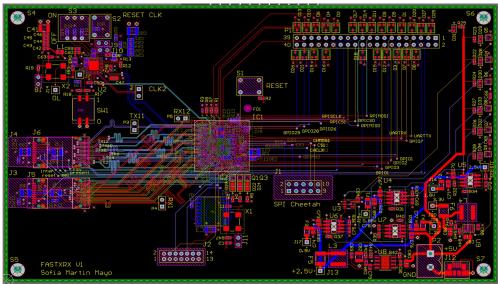




Prototype 2: CTP high-speed testbench

- Building the testbench
 - Firefly optical transceiver + Microwave PCB + FPGA interface.
 - Test the capabilities and quality of the companies to produce the final board.
 - Design finished and files sent to the manufacturing company.









AI for CTAO DVR



CTA Offline Data Volume Reduction: Al algorithms on GPUs

Status

- Prior experience in IACT event reconstruction (LST-OnSiteAnalysis) using AI (CTLearn)
- Applying analogous CNN algorithms to address the challenge of offline Reducing the CTA Data Volume ← *Data Rate* x *Data size*
- Integrate AI capabilities into the CTA offline analysis pipeline, seeking a more efficient processing chain in both computational and storage aspects
- Initial activities fostered after AI for CTAO Trigger activities
- Contribution needed in 2025-2028





AstroHEP PPCC impact



Scope

- ~90 k€
- Engineer costs: A. Pérez-Aguilera, May 2023 March 2025

Impact







- Current design and prototyping of a SiPM-CAM key element
- Allow to apply for other grants (PDC2023

 ✓ , EU INFRA-Tech
- Transfer of knowledge started for fast Al-based image processing on FPGA

Plea

4-month extension



Summary



