# Advanced Instrumentation for future colliders

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# Instrumentation for Future Colliders

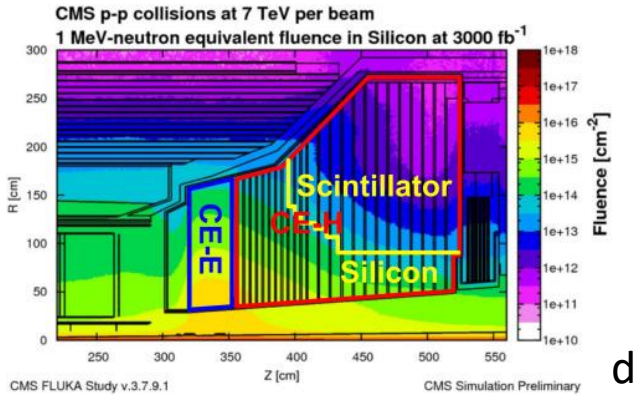
The instrumentation for future colliders will be grounded in the developments currently underway for HL-LHC:

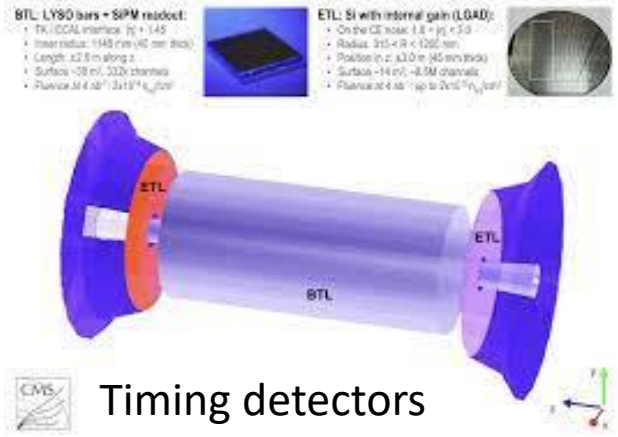
HL-LHC conditions require significant upgrades of the detectors.

- Radiation hardness. Silicon based detectors. Cooling around -30º C.
- Mitigate physics impact of high pileup. ~30 ps MIP timing resolution.
- Higher resolution and granularity to reduce occupancy.
- Increase geometrical coverage.
- Higher data rate, improved trigger algorithms and more intelligence into the detector

Examples of those are:

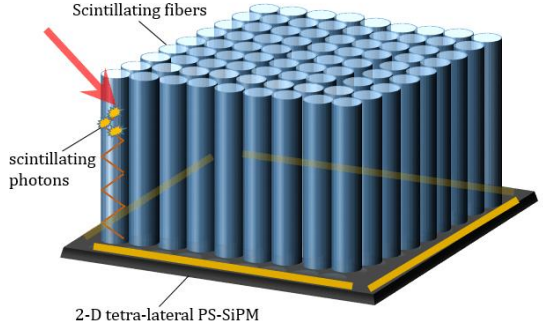
High granularity calorimeters



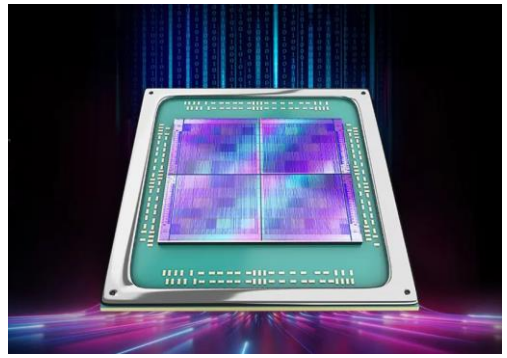




Timing detectors

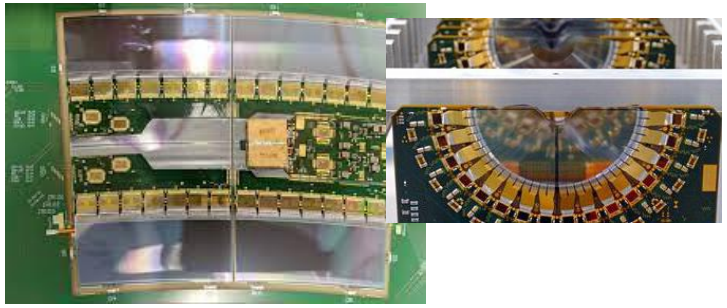
Fiber trackers, SiPM



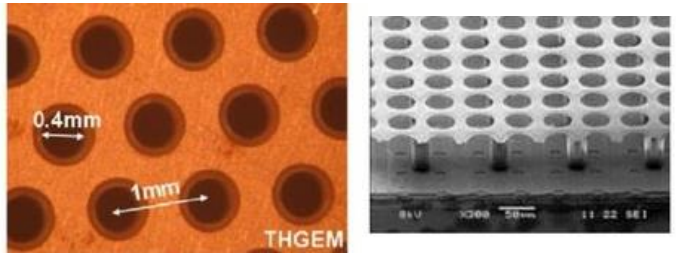

Trigger, triggerless



Novel Silicon detectors



Novel gaseous detectors



# Instrumentation for Future Colliders

Future colliders and technology trends:

- At FCC-ee or any e+e- machine, it is likely that radiation hardness turns into a less severe constrain
- But we will profit to address other challenges such as improved granularity and resolution.

The design of **high-performance electronics** is particularly relevant to address the rest of these challenges, by allowing to exploit the maximum capabilities of the detector using the **latest technological developments in microelectronics, optoelectronics and reconfigurable hardware.** This will be common mantra for all detectors.

At **CIEMAT** we are:
Leveraging our expertise of the electronics that we are developing for the **HL-LHC upgrade**, key areas appear as the most promising to expand our R&D:

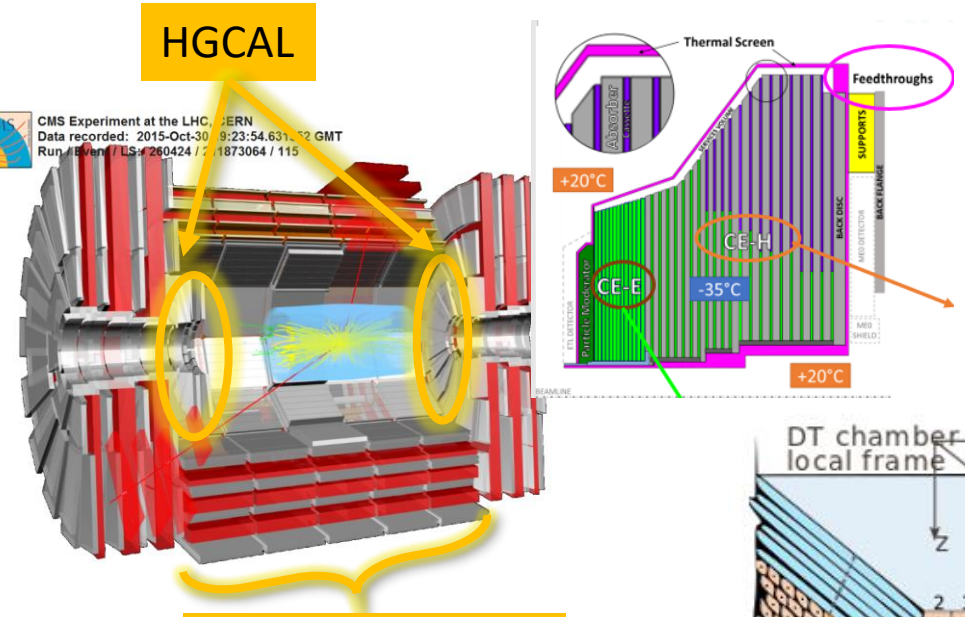
- Construction of **high granularity calorimeters**
- **Improve timing** in particle physics detectors and particularly, time distribution techniques
- Bringing **intelligence to the detector**
- Novel **readout and digital trigger** architectures

This is happening within the framework of the **CMS** collaboration, **CALICE** collaboration, **Detector R&D** collaborations hosted at CERN (DRD1 DRD6, DRD7)

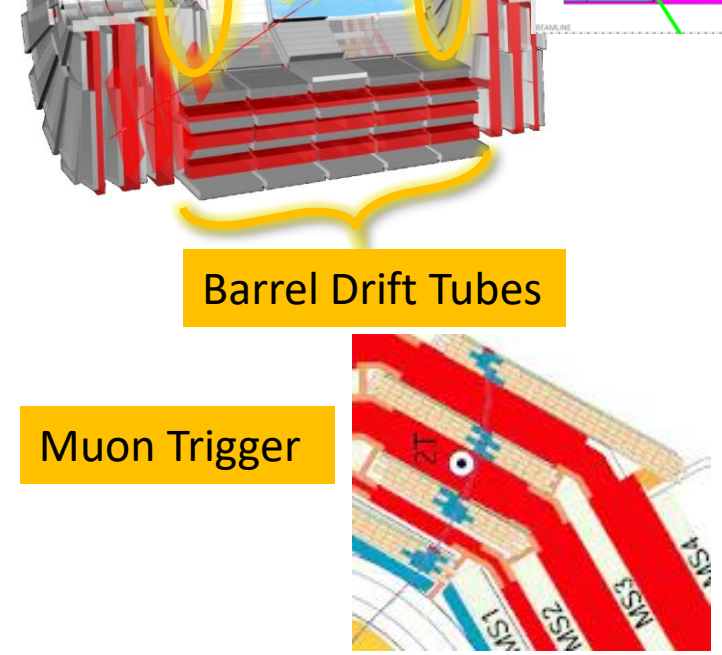
# CIEMAT @ the CMS HL-LHC Upgrade

- 250 chambers to be refurbished with new electronics:
  - Time digitization of the 172200 channels
  - Chamber interfaces, pressure ADCs, alignment forks, RPC interfaces, etc
- 830 boards embedded in the 250 Minicrates structures
- Full refurbishment of backend electronics with improved performance

HGCAL

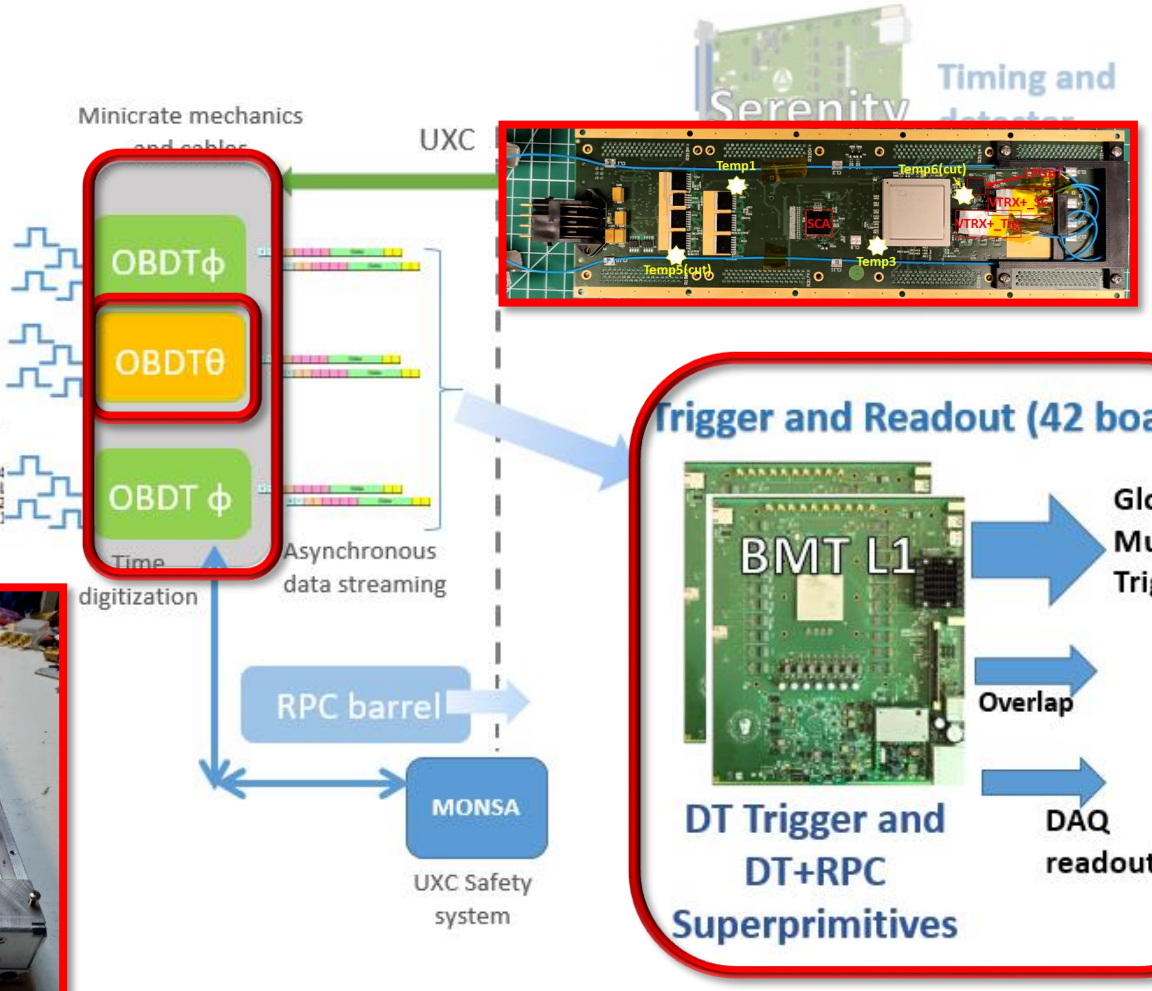



Barrel Drift Tubes




Muon Trigger




- Radiation tolerant electronics (theta view)
-Mechanics and cabling
-Backend hardware
- Muon trigger algorithm and firmware
-HGCAL mechanics and interfaces

**CIEMAT**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AGENCIA ESTATAL DE INVESTIGACIÓN
Plan de Recuperación, Transformación y Resiliencia
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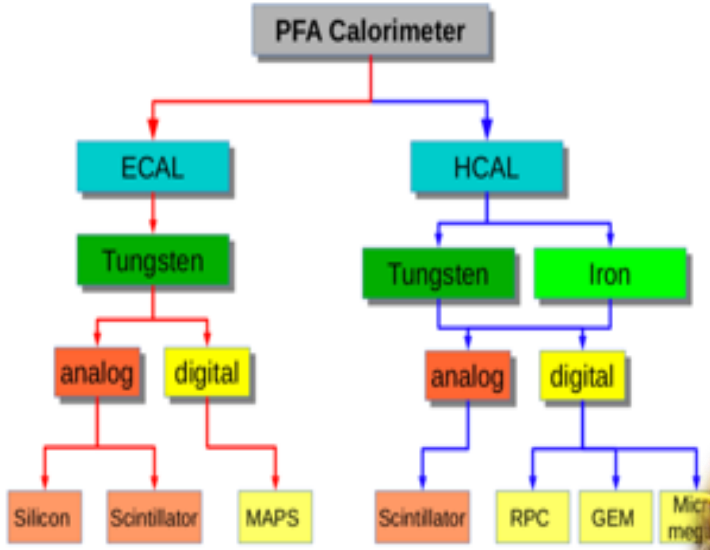
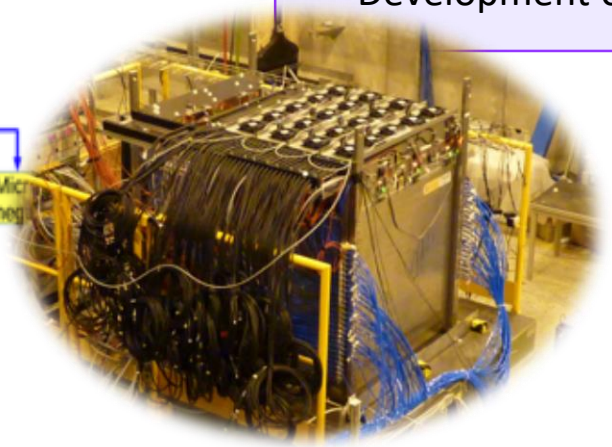
# R&D on highly segmented calorimeters – CALICE & ILD

*R&D on highly granular calorimetry optimized for particle flow event reconstruction*

*Sampling calorimeters under CALICE development*




SiWECAL SDHCAL



**1m³ prototype**
**~500K channels**

From M.C.Fouz

## SDHCAL:

*Absorber: Stainless Steel + Detector: Glass Resistive Plate Chambers*
*Semi-digital readout with **1cm²** pads*

CIEMAT is one of the major contributors with **responsibilities on:**

- Mechanics
  At present, developments on welding for large mechanical structures
  Electron Beam Welding (EBW) and Laser Welding
- Electronics
  Readout boards: design of the DIF board
- Test beams, data analysis and Monte Carlo
  Development of algorithms, reconstruction and test beam data analysis

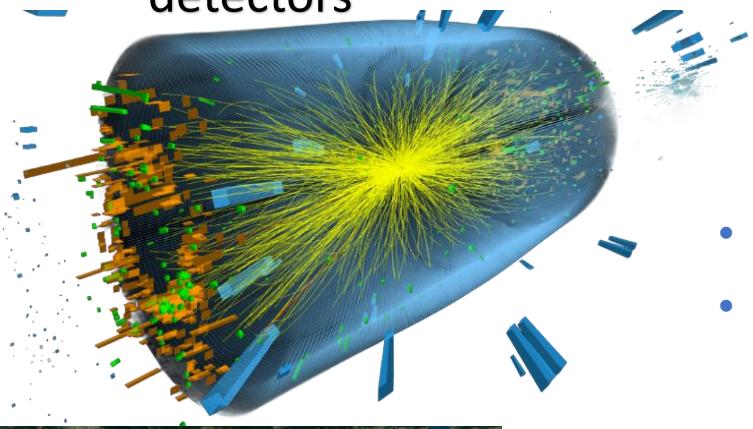
## SiWECAL

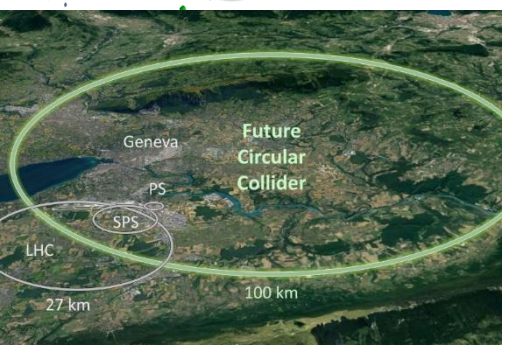
*Absorber: Tungsten + Detector: Silicon Sensors*
*Analog readout with **5x5 mm²** pads*

**Participation on** test beams and data analysis
Detector alignment and MIP callibration

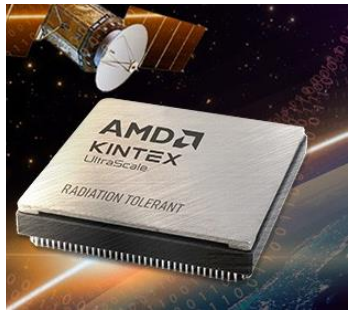
# Intelligence on detector

Particle collider detectors






- Technology trend is to bring larger amount of **intelligence near the detector**, allowing intelligent techniques:
  - Discriminating signal/noise, signal shape, geometry, PID,
  - Time measurement, switching matrixes, handling of large throughput
- **Programmable logic** allows implementation of diverse algorithms and also, modification
- In general FPGA performance is worse than ASIC's regarding radiation and power but it has **big advantages in terms of developing time and reusability**
- In LHC detectors, trade off typically restricted FPGAs to the outside areas of the detector, typically Muons.
- In detectors for e+e- colliders the **boundary of usability due to radiation moves significantly towards the IP** (no hadrons, only TID).
  - For instance, Alice inner Tracker CMOS MAPs, a technology considered for FCC-ee, spec is [700krad, 10krad]

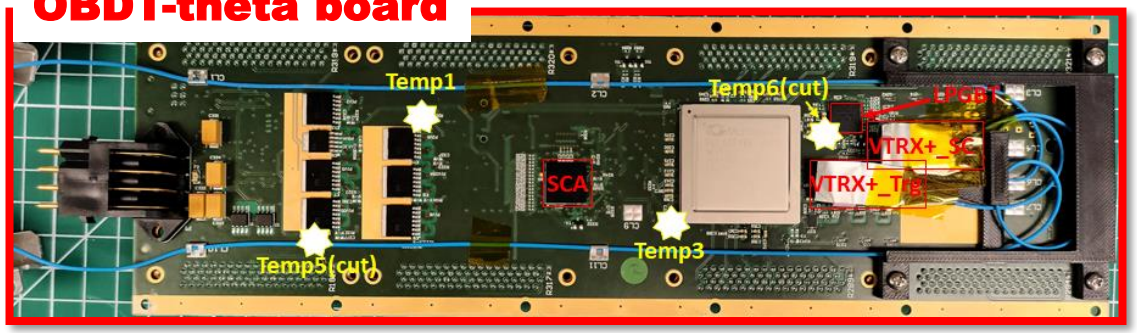




- This may open the door to using **commercial FPGAs in larger areas of the detectors**
- Microchip has in the market the **PolarFire technology of Flash based FPGAs** adequate for mild levels **(<3000Gy)**

# Intelligence on detector under mild radiation

- CIEMAT has designed a board around the **Polarfire FPGA**
- It is a board with **228 time digitization channels** (0.7ps)
- Designed for a mild radiation environment using COTS
- Large throughput through optical links **61,44 Gbps**
- 14 layers, halogen free material

**OBDT-theta board**




- We have tested under **radiation at CHARM** (CERN) with a high energy hadrons mixed field for 100 Gy
- **Very good results by the FPGA**, comparison with published reports
- Also relevant information regarding the **poor performance of commercial optical transceivers**

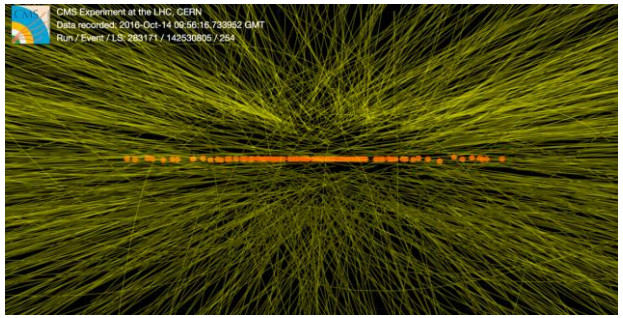
| | Our test | PSI CERN | Microsemi LANL 2018 |
|---|---|---|---|
| | Cross-section (cm2/bit) | Cross-section (cm2/bit) | Cross-section (cm2/bit) |
| CKBD 40 MHz | 2,27E-14 | 2,66E-14 | 1,47E-14 |
| CKBD 10 MHz | 1,00E-14 | 2,31E-14 | 2,09E-14 |
| FF All 1s | 6,23E-15 | - | 7,39E-15 |
| FF All 0s | 8,83E-15 | 5,31E-15 | 7,39E-15 |
| LSRAM SEUs | 1,15E-14 | 1,37E-14 | 1,42E-14 |
| LSRAM MBUs | 9,55E-19 | < 9,5e-18 | 5,58E-16 |

**Irradiation at CHARM**

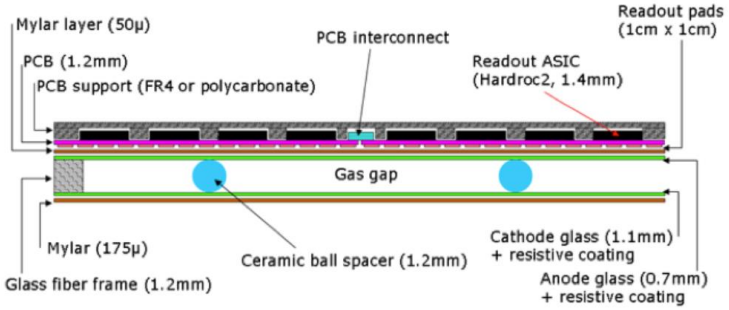
# Timing, the tens of picoseconds regime

Electronics timing resolution is very good since a while
Novelty is that recent detectors can achieve very good timing, and this can be very useful:

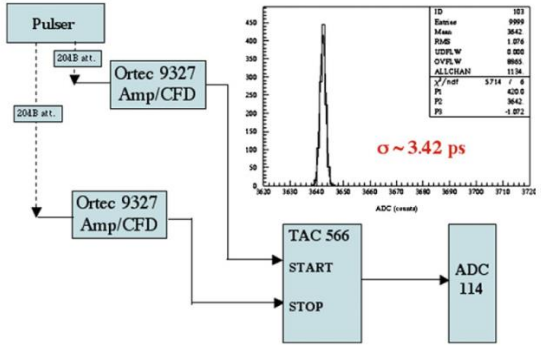
- TOF
- PID
- Vertex id
- Particle flow




MTD at CMS




Glass RPC (CALICE)




- Electronics timing resolution is very good since a while
- The challenge is to replicate it over many channels

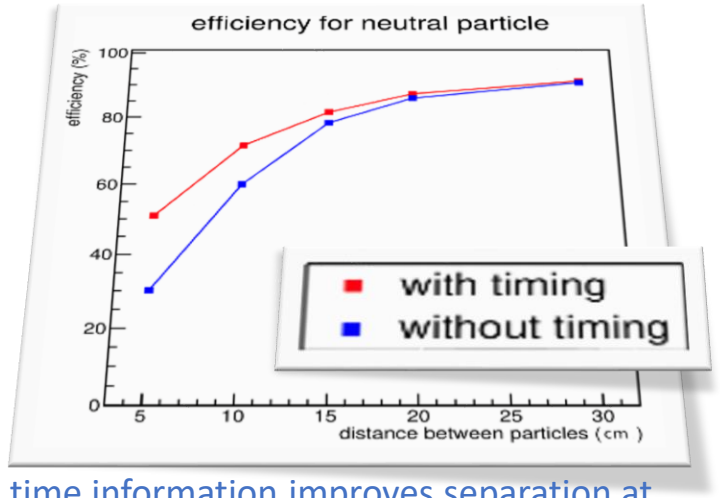
A. Rivetti (INFN-Torino) | IC for precision timing | Ps workshop,


- Challenge is to bring this capability to **many channels in a large detector**
- Present goals: improve time resolution **well below 100 ps** (target 10 ps or less)
- Extend timing to **densely packed detector systems**
- Impedance control, front end matching
- Make large detectors **cheaper**

# Timing at Calorimeters

Calorimeters case

- Calorimeters already achieve quite good time resolution
- System resolution now saturates at around 100 ps
- Exact values depends on the situation considered
- Interaction region ≈ 6 cm
- With 30 ps resolution event origin confined to 1 cm.
- Need a 4-5x improvement with respect to today standard



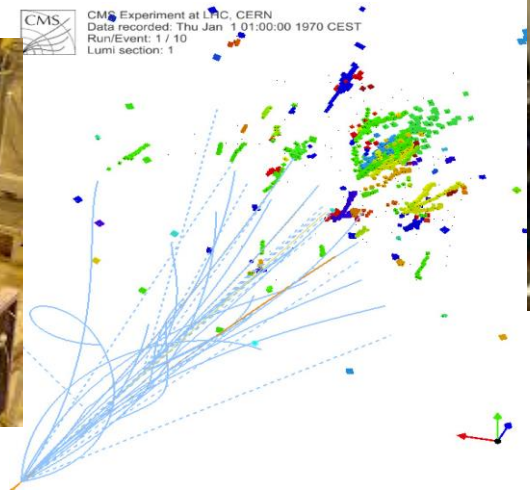

time information improves separation at lower distances.

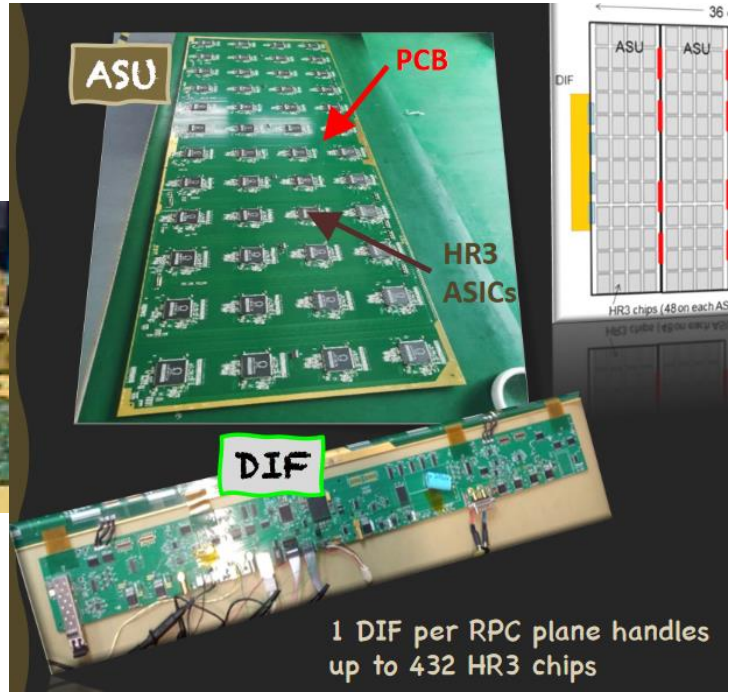
**General t-SDHCAL goal**

Extending the Semi-Digital Hadronic CALorimeter (SDHCAL) to include timing information (100-200ps resolution) for a 5D-calorimetry (space, amplitude & timing)

**Implementation**

Build multi-gap RPC (MRPC) equipped with a new version of electronics with timing capabilities to prove the final performance



# High precision timing: timing distribution

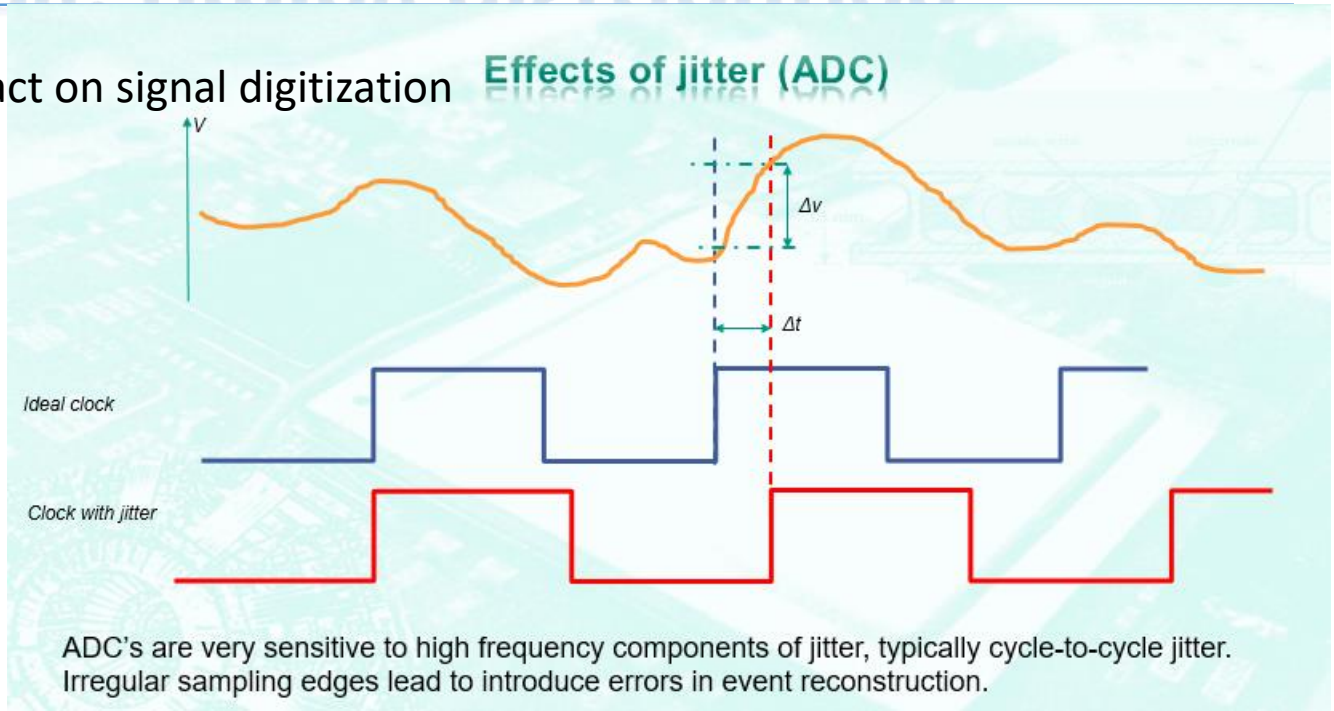
Timing involves several critical processes:

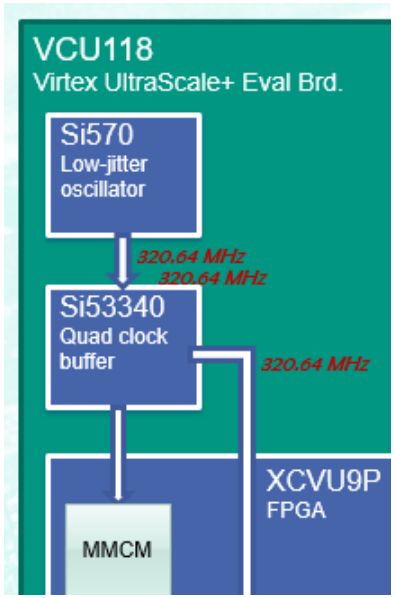
- Signal generation in the **sensor**
- Signal processing in the **front-end electronics**
- **Clock distribution** to the whole detector

Time distribution needs to be kept under control

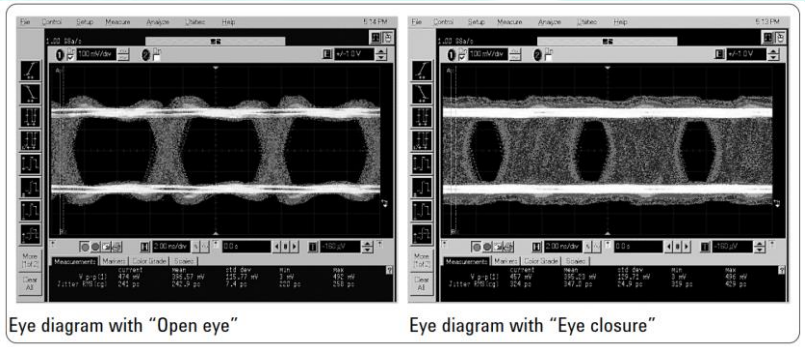
- **Jitter**: deviations from a fixed clock frequency. Critical in analog to digital conversion phase. Every item in the clock chain can introduce jitter and needs to be kept under control

Impact on signal digitization



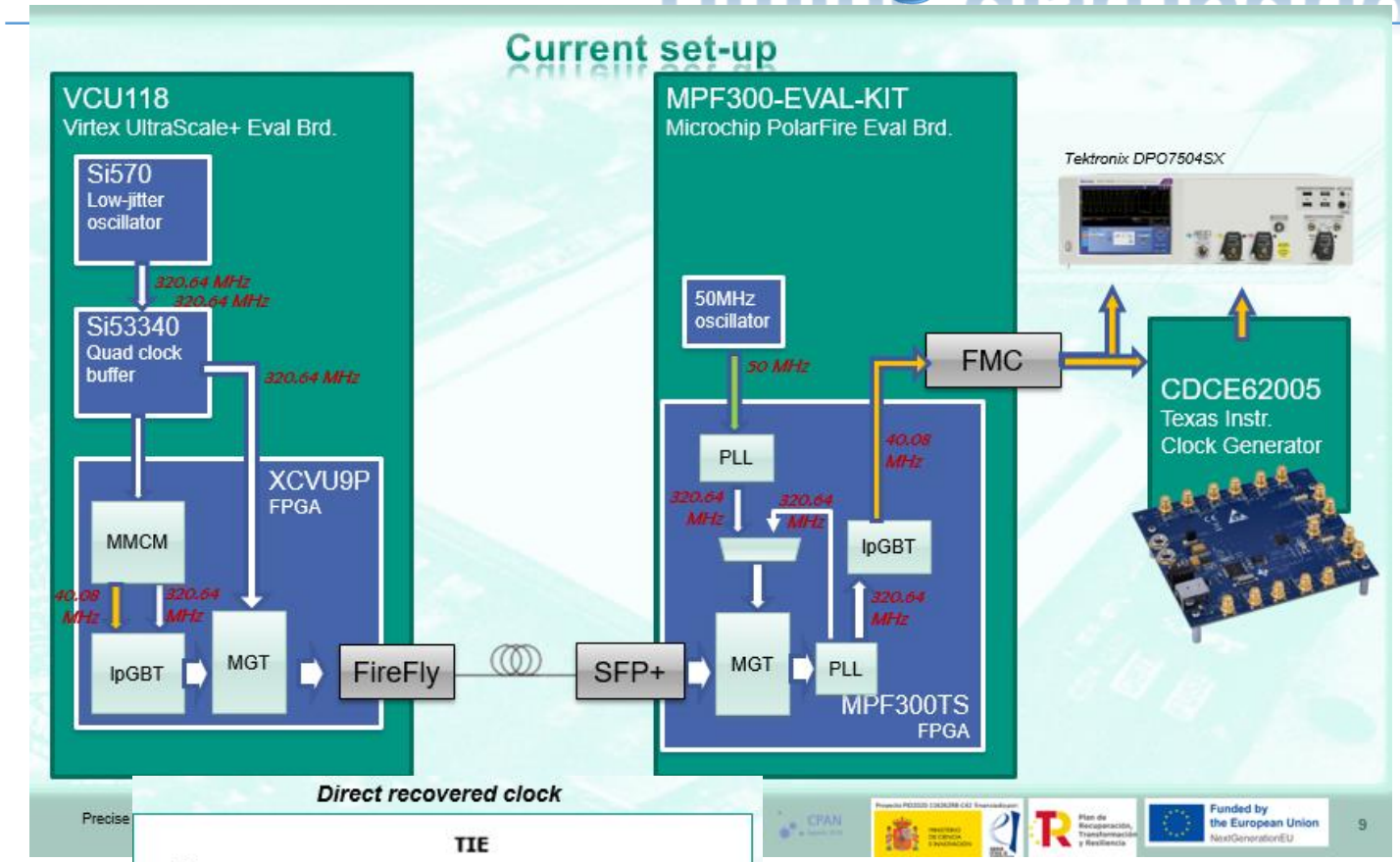

- **Phase**: system needs to be robust against configurations/power cycles/clock glitches
  - Intense effort in CMS Phase 2 to maintain this under control in the clock distribution chain which is based on FPGAs and PLLs
  - In our case, special firmware developed for reliable operation on the various FPGAs (Polarfire, Virtex 7, Virtex Ultrascale+)

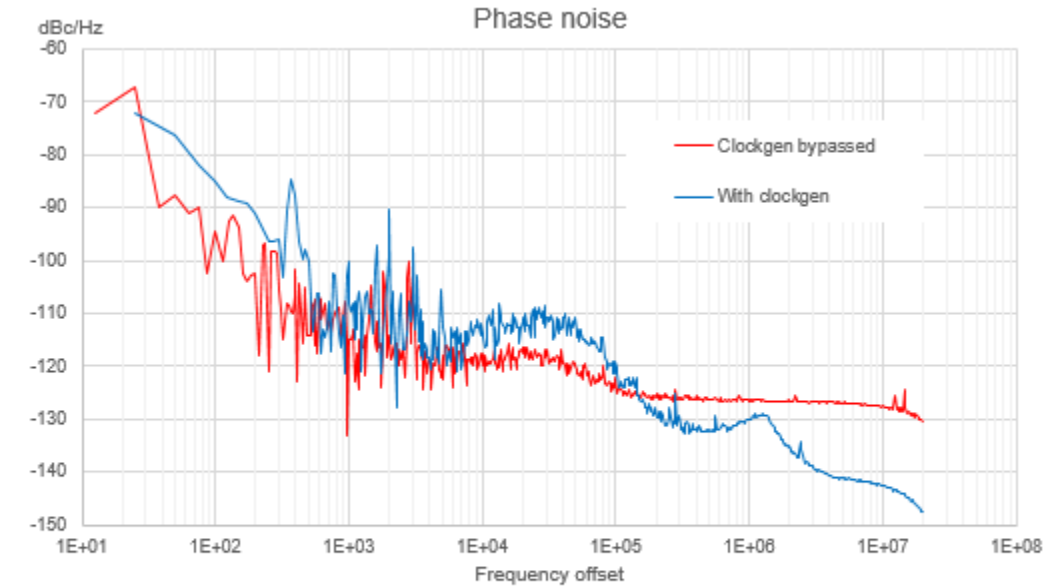


Eye diagram with "Open eye"

Eye diagram with "Eye closure"

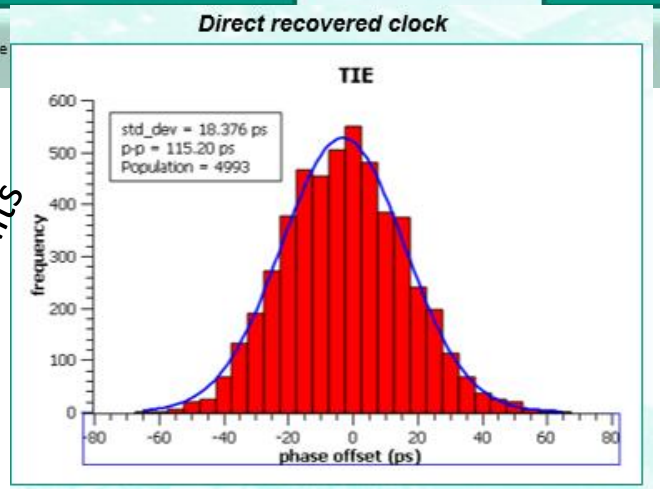
# Timing distribution studies




The phase noise of a real clock is a random modulation of the phase of the ideal signal.
It quantifies the **fluctuations in the timing** of the signal's phase.

Early results




- Virtex Ultrascale+ evaluation board for 320 MHz with a low-jitter oscillator for reference
- Polarfire evaluation board is used as intermediate clock step in a clock chain.
- Clock needs to be recovered and its quality evaluated
- The recovered clock is directly measured with the scope and also is used as an input of a clock generator, whose output is measured as well.

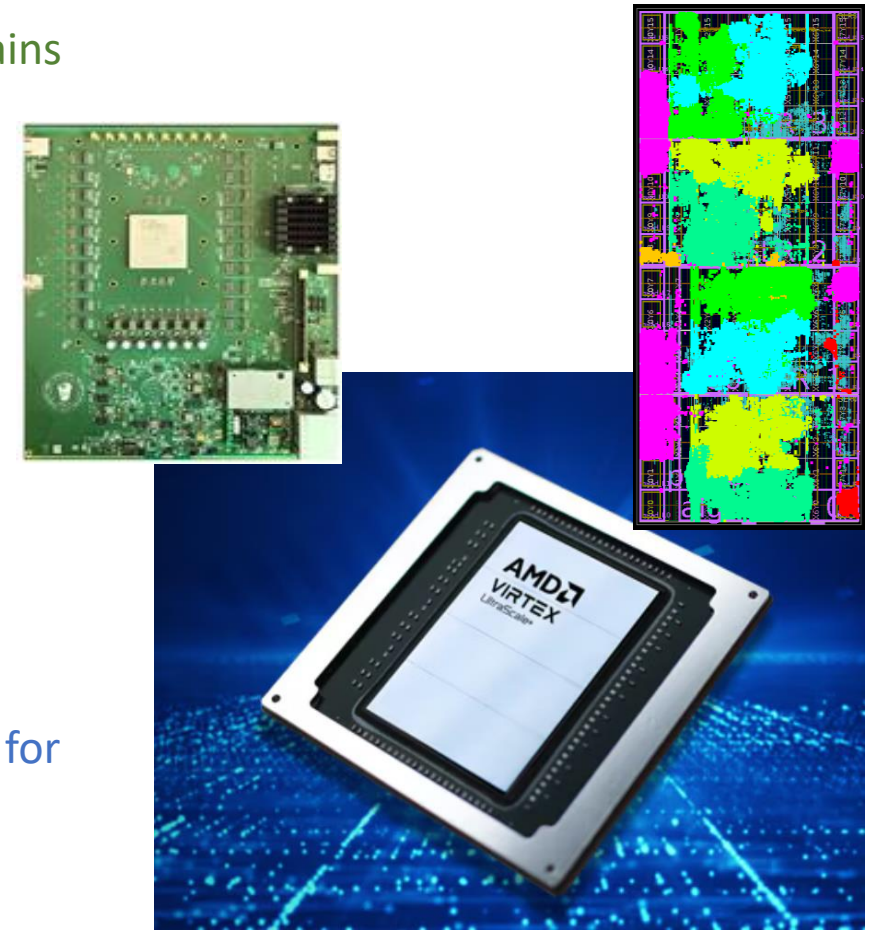
# Intelligence outside the detector

Evolution of the digital electronics offers the possibility of moving important parts of complex algorithms to the hw system

Traditionally, and particularly important in hadronic colliders as luminosity increases, a trigger system was mandatory to cope with the bandwidth. Future is **triggerless**?

Necessity for **fast information processing** and implement **complex algorithms** remains

Increasing granularity and resolution will only make this need more pressing




At CIEMAT we have been working since several years on the implementation of the **muon barrel trigger primitive generation algorithm**

- https://doi.org/10.48550/arXiv.2302.01666
- **Achieved offline performance at Level 1 trigger**
- Developed the firmware in various platforms: Virtex 7, Virtex ultrascale +

- Implementing machine learning techniques inside the firmware, the use of HLS for easing physics to fw effort, use of AI dedicated programmable devices
- Edge computing, neuromorphic computing, etc

# Intelligence outside the detector

- The evolving COTs technologies and its performance needs to be considered for real-time backend processing
- We are working now in the **benchmarking** of heterogeneous COTs architectures and in the development of TDAQ tools.
- Throughout the years, we have developed plenty of highly-optimized (**latency, resources, throughput**) modules for FPGA which could be of interest for the community

Some examples:

- **Implementation of a piecewise approximation to an arbitrary function**
  - Automatic input range partitioning and sizing of fixed-point coefficient widths for a target approximation error.
  - HDL implementation uses of DSP and RAM, highly pipelined, high clock frequency.
  - Example: coordinate conversions using complex trigonometric relationships
- **Multivariate linear regression of a set of data points with quantized independent variable(s)**
  - Automatic sizing of fixed-point coefficient widths for a target resolution.
  - HDL implementation uses DSP & RAM, highly pipelined, high clock frequency. Outputs parameters, residuals, sum of squared residuals
  - Example: DT segment fit (z fixed for each layer), detections at fixed time intervals, fixed distances…
- **Sparse input serializer: serialize data from parallel source with sparse occupancy**
  - Automatic selection of optimum architecture depending on parameters (clock frequency, input/output widths…), option for radiation environment (TMR, RAM ECC)
  - Examples: on-detector readout of high-granularity, low-occupancy detector; also useful as submodule in algorithmic block for queuing “hits” from a combinatory stage.
- **Several other smaller modules, some LHC-specific or CMS-specific**

Made available to DRD7.5 collaborators

# Summary

At CIEMAT we are working on the R&D on detector and electronics in view of future experiments

We are leveraging our expertise in CMS and Calice:

- Construction of **high granularity calorimeters:** important effort in the **construction of Calice** prototypes and **present participation in CMS HGCAL**
- **Improve timing** in particle physics detectors and particularly, **time distribution techniques**: work in the tens of picoseconds regime for a large detector.
- Bringing **intelligence to the detector: developed expertise on FPGA firmware development for complex algorithms**
- Novel **readout and digital trigger** architectures: design and construction expertise

We are exploiting the expertise on one of the latest **FPGAs** in the market that is adequate for **radiation environments**

Studies on clock distribution systems that could be capable of providing ultimate timing precision are preliminary but the **setup and methods have been developed.**

Work in on going on **cutting-edge programmable logic for implementing intelligent algorithms** directly at the detector level offering real-time data analysis capability. We are working in collaboration with international developers for **sharing code and developments**